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RADIATION INFLUENCE ON ELECTRICAL CHARACTERISTICS OF COMPLEMENTARY JUNCTION FIELD-EFFECT TRANSISTORS EXPLOITED AT LOW TEMPERATURES

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Abstract. Computer simulations of fabrication processing p-and n-channel junction field-effect transistor with design norms of 1.5 μm is presented. Corrections to parameters of Klassen mobility model are proposed. They ensure the correspondence between calculated current-voltage characteristics and experimental data. For the investigated device structures of JFET, an analysis of the influence of various types of penetrating radiation on electrical characteristics is carried out. Optimization calculations gave the modes of processing procedure, which reduce the effect of the neutron flux with energy 1.5 MeV on the electrical characteristics of n-JFET device structure by 1.45 times.

Keywords: computer simulation, current-voltage characteristic, field-effect transistor, neutron, radiation

1. Introduction

Influence of radiation penetrating in semiconductors and structures with p-n-junctions is manifested in radiation defects [1-3]. In addition to the negative impact, penetrating radiation can serve as an effective technological tool that allows obtaining qualitative semiconductor materials, significantly improve and cheaper production of semiconductor devices [4, 5]. A technological manufacturing semiconductor device uses many types of penetrating radiation: fast electrons, gamma radiation, neutrons, protons, alpha particles, etc. Modeling electrical characteristics that takes into account different radiation types is an actual task aimed at improving the performance characteristics of integrated circuits (IC). The task solution with the purpose of creating microelectronic radiation-hardened hardware components and the development of special circuitry has received increased attention [6, 7].

Synthesis of high-quality analog of IC that are low-sensitive to the action of penetrating radiation is advisable to perform on bipolar transistors (BT) and junction field-effect transistors (JFET) with a large boundary frequency [8, 9]. In Ref. [6], the investigation results of the hardness of ABMK version 1_2, (JSC "INTEGRAL", Minsk) are given, which show that the highest hardness is possessed by p-JFET, and the smallest by side p-n-p-transistors. The hardness of JFET is explained by the fact that their functioning is caused by the motion of carrier majority far from the surface, so the radiation-induced alteration of surface state has no significant effect on its parameters.

2. Structure of p-channel JFET

JFET belongs to the category of normally open field-effect transistors in which the conducting channel and, therefore the current in the channel close to maximum, exists at a

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zero potential on a gate ($V_G = 0$). These JFETs are called devices of a depleted type, since when the voltage is applied to the gate, the channel is depleted by electric current carriers and the current in the channel decreases.

The device structure of the p-channel junction field-effect transistor studied is shown in Fig. 1, a substrate being of hole conductivity type, boron-doped with concentration $1.35 \cdot 10^{15}$ cm^{-3}, crystallographic orientation (111). Modeling the formation of p-channel JFET structure, 14 steps are conventionally identified: setting the substrate parameters and selecting the reference grid, sequential formation of areas: n^+-buried layer, p^+-buried layer, epitaxial layer, oxide insulation, p-well areas, n-collector, p^+-collector, p-base, areas opening for contacts (together with oxidation of the substrate surface), creating regions of n^+-gate, p^+-emitter, n^+-emitter, 1st level of metal interconnections. To form the structure, 11 operations of photolithography are necessary.

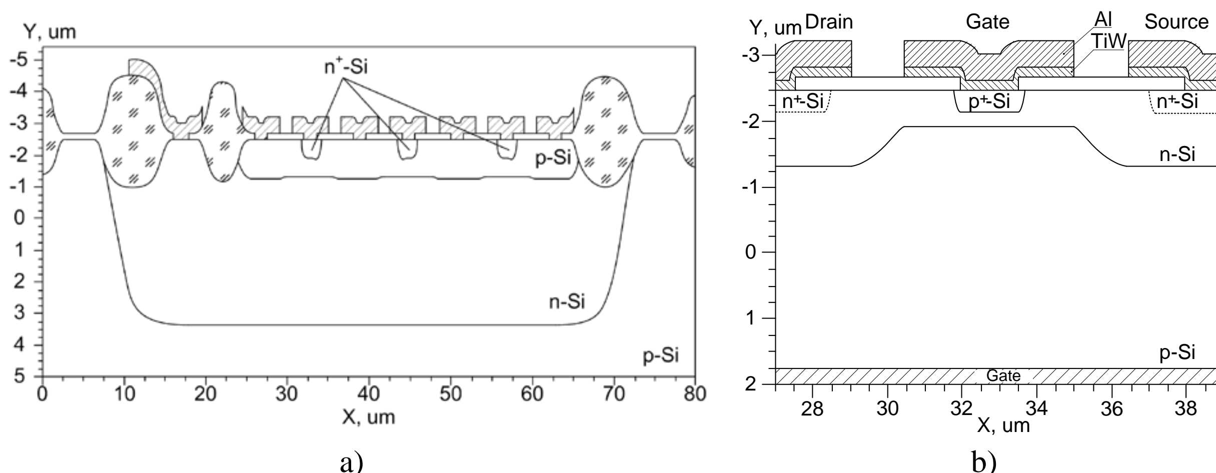


Fig. 1. Device structure of p-channel (a) and n-channel (b) JFET

It has been established by computer simulation that the application of carrier transport models, which take into account the dependence of semiconductor parameters on the temperature available in the software complex, does not ensure the convergence of the results with a full-scale experiment. The closest values of electrical parameters were obtained using the mobility analytical model and the Klassen mobility model. Based on the results of computer modeling, the Klassen mobility model was chosen as the basic model. Figs. 2 and 3 show the results of modeling.

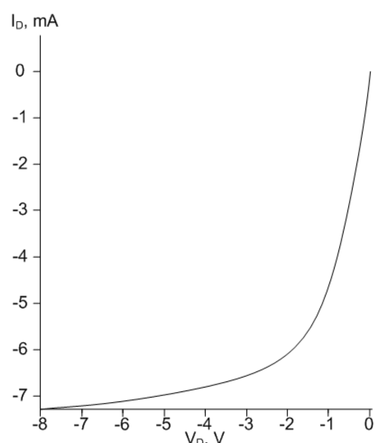


Fig. 2. Dependence of drain current I_D on drain voltage V_D at T = 303 K

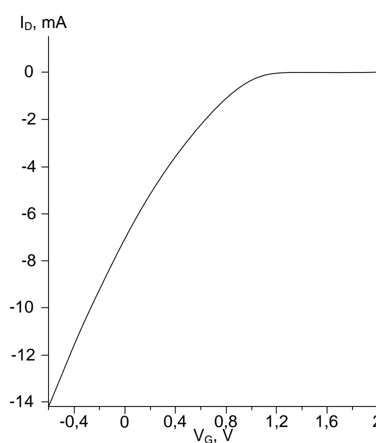


Fig. 3. Dependence of drain current I_D from gate voltage V_G at T = 303 K

3. Temperature freezing-out of impurities

The conditions for the application of the JFET require studying the impact of penetrating radiation over a wide temperature range (from 163 to 383 K). In a nongenerated donor semiconductor at absolute zero temperature, the Fermi level is located halfway between the bottom of a conduction band and the donor impurity level. At sufficiently low temperatures (several degrees of Kelvin), the Fermi level initially rises to a certain maximum value, and then begins to decrease and takes on values, just as for the case T = 0 K. Such a shift of the Fermi level corresponds to an exponential temperature dependence of the electron concentration. This region of Fermi level change corresponds to the region of weak impurity ionization (freezing-out region).

With further temperature increasing, the electron concentration in the conduction band becomes comparable with the impurity concentration, wherein practically the entire donor impurities are ionized, so the electron concentration does not depend on temperature. This temperature range, at which cumulative impurity ionization occurs, is called the impurity depletion region (region of cumulative impurity ionization). Further temperature increasing raises the electron concentration in the conduction band due to electron transitions from the valence band (intrinsic conductivity region).

A model of partial ionization is used for simulating the temperature freezing-out of impurities in silicon at high impurity levels, which gives acceptable physical results for low and medium impurity concentrations. However, for values of impurity levels greater than $3 \cdot 10^{18}$ cm^{-3}, this model poorly describes experimental results. For increasing the result convergence of computer and full-scale experiments, and also for using it in a wider temperature range (up to 70 K), several options have been proposed: application of the modified Klassen mobility model, development of a simplified model mobility based on materials of the full-scale experiment of PADJ structure; joining the modified Klassen model and additional models (Incomplete, Ioniz).

Modified Klassen mobility model. Simulation allows find the parameters that have the greatest influence on current-voltage characteristic of p-channel JFET (coefficients of model). The results obtained with these parameters are presented in Table 1 and Fig. 4.

Simplified mobility model. Due to the lack of measurement results for temperatures below 223 K, the data obtained by measuring the analog of device structure (PADJ) are taken as a basis. The calculated results are shown in Fig. 5.

Modified Klassen model together with Ioniz model. The use of additional impurity ionization models (Incomplete, Ioniz) requires changing the Klassen mobility model. Despite the decrease in deviation at low and high temperatures, the analysis shows that changing only four parameters of the model is insufficient for correct description of the electrical characteristics over a wide temperature range (from 73 K to 383 K). An optimization calculation was carried out for all parameters of the Klassen mobility model responsible for hole mobility (26 parameters). As the cost function, the drain current value I_D is used at the gate voltage $V_G = 0$ V, at the drain voltage is $V_D = -3$ V, obtained as a result of the full-scale experiment, and predicted by the previous method (data for PADJ). Comparison with the full-scale experiment is presented in Table 1 (simulation #3). Figure 6 shows the electrical characteristics of the p-channel JFET, calculated with optimized parameter values.

Table 1. Comparison of full-scale experiment and computational results

Temperature,	Pinch-off voltage V_{Goff} at $I_D = 1$ μA, V				Drain current at $V_{GS} = 0$ V, $V_{DS} = -3$ V, mA			
K	meas.	mod. #1	mod. #2	mod. #3	meas.	mod. #1	mod. #2	mod. #3
223	1.15	1.165	1.154	1.143	4.4	5.19	3.15	4.88
303	1.29	1.299	1.298	1.31	3.345	3.69	2.90	3.82
383	1.425	1.485	1.486	1.484	2.674	2.91	2.75	2.94

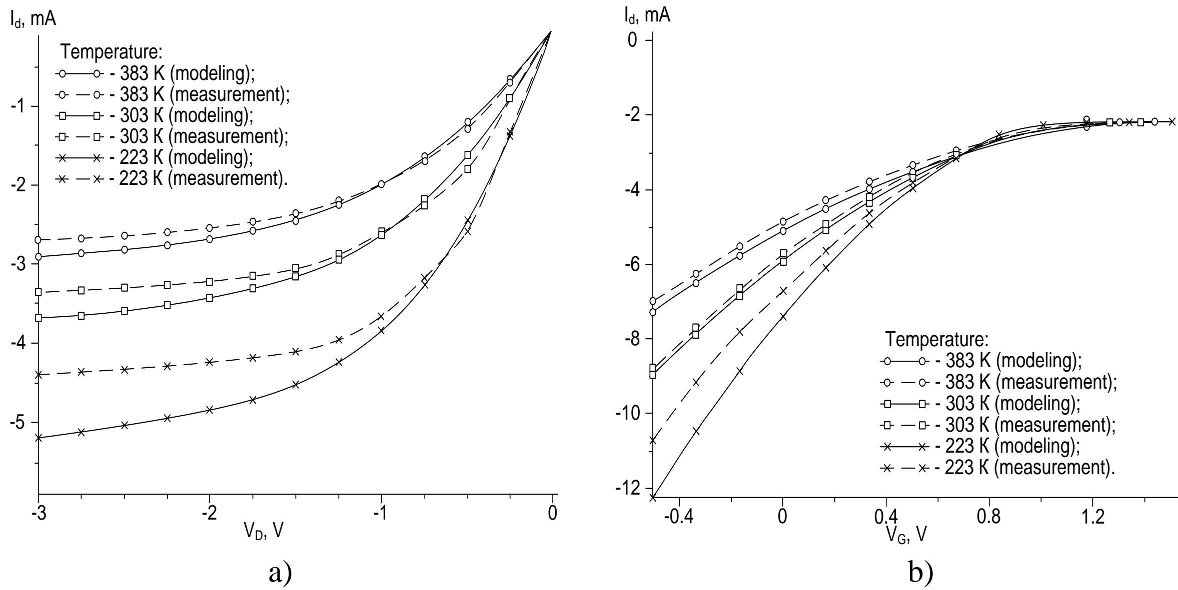


Fig. 4. Dependence of drain current I_D from drain voltage V_D at gate voltage $V_G = 0$ V (a) and drain current I_D from gate voltage V_G at drain voltage $V_D = -3$ V (b)

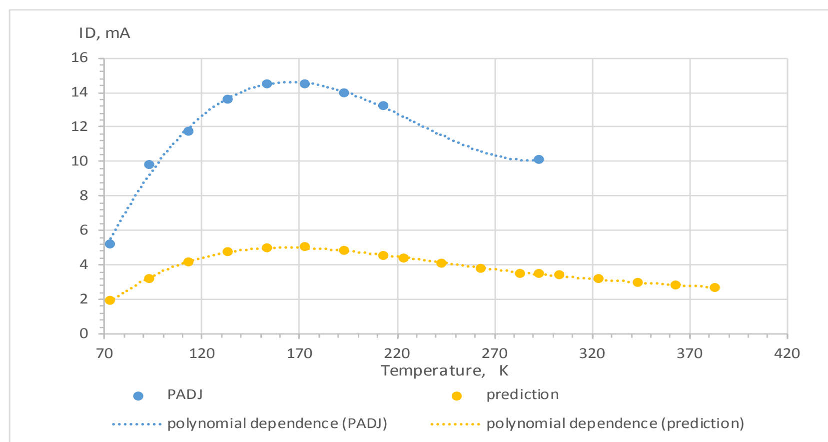


Fig. 5. Dependence of drain current on temperature for PADJ structure (blue curve) and for p-channel JFET structure (yellow curve)

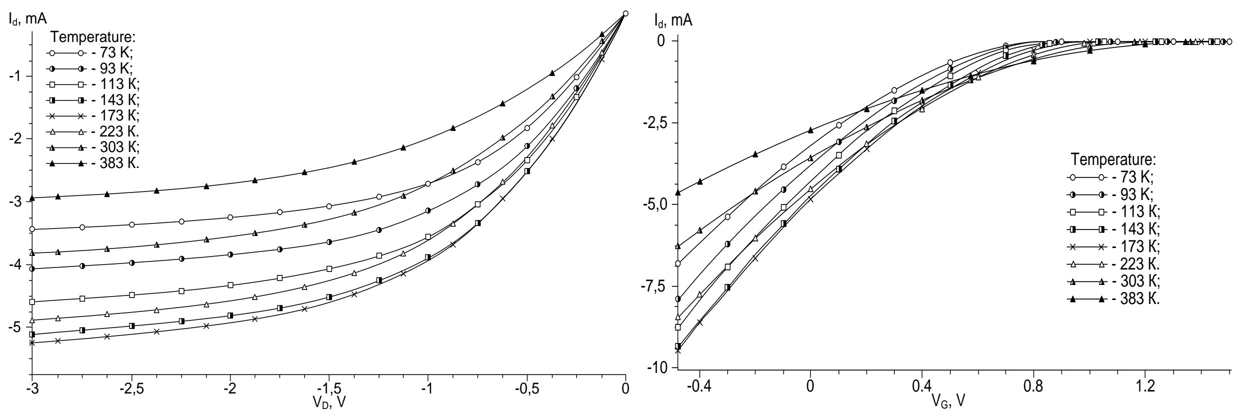


Fig. 6a. Dependence of drain current I_D on drain voltage V_D at gate voltage $V_G = 0$ V

Fig. 6b. Dependence of drain current I_D on gate voltage V_G at drain voltage $V_D = -3$ V

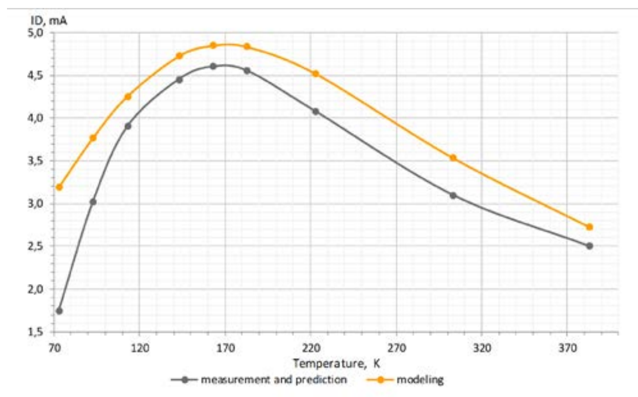


Fig. 7. Dependence of drain current I_D on temperature at drain voltage $V_D = -3$ V and gate voltage $V_G = 0$ V

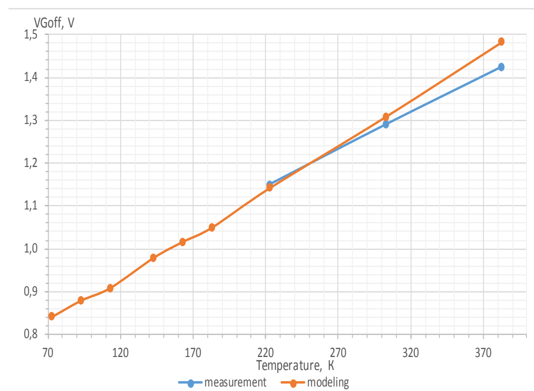


Fig. 8. Dependence of pinch-off voltage V_{Goff} on temperature at drain voltage $V_D = -3$ V and drain current $I_D = 10^{-3}$ A

4. Modeling the effect of penetrating radiation

As shown in Ref. [10], there is a combination of fluence and particle energy values at which the radiation effect is equal. It is assumed that the electron fluence F_E with energy $E_E = 4$ MeV creates the same displacement defects in the IC as the neutron fluence $F_N = 0.302 \cdot F_E$ with energy $E_N = 1.5$ MeV or the proton fluence $F_P = 1.1 \cdot 10^{-4} \cdot F_E$ with energy $E_P = 2.0$ MeV. Figure 9 shows the action of the electron fluence $F_E = 6 \cdot 10^{14}$ cm^{-2} with energy $E_E = 4$ MeV and of corresponding neutron and proton fluence at temperature $T = 303$ K and gate voltage $V_G = 0$ V.

From this figure we notice that the irradiation with the parameters mentioned above produces practically identical changes in the device electrical characteristic. Thus, the drain current of p-channel JFET under radiation by the electron fluence $F_E = 6 \cdot 10^{14}$ cm^{-2} with energy $E_E = 4$ MeV reduces by 5.7 % with respect to that of JFET without radiation ($I_D = 3.70$ mA and $I_D = 3.49$ mA, respectively). For the neutron fluence $F_N = 2 \cdot 10^{14}$ cm^{-2} with energy $E_N = 1.5$ MeV, the change is 4.6 % (drain current value $I_D = 3.53$ mA). For the proton fluence $F_P = 6.6 \cdot 10^{10}$ cm^{-2} with energy $E_P = 2$ MeV, the change is 4.9 % (drain current value $I_D = 3.52$ mA).

Figure 10 shows the dependence drain current on the electron fluence F_E with energy $E_E = 4$ MeV at different temperatures. The drain current is expressed in relative units, the value of drain current without radiation being unit. From the figure one can see that at temperature $T = 383$ K and electron fluence $F_E = 2 \cdot 10^{15}$ cm^{-2}, the drain current is 88 % of that value without radiation, at fluence $F_E = 6 \cdot 10^{15}$ cm^{-2} its value is 67 %. At temperature 223 K, the drain current drops to 79 % and 45 % for fluences $F_E = 2 \cdot 10^{15}$ cm^{-2} and $F_E = 6 \cdot 10^{15}$ cm^{-2}, respectively. With further decreasing temperature to 163 K, drain current diminishes to 64 % and 26 %. It can be concluded that decreasing temperature increases the electron radiation impact. This is connected with the annealing of crystal structure at higher temperatures. Analogous results were obtained in the case of neutron (Fig. 11) and proton (Fig. 12) radiation.

Figure 13 shows the results of modeling dynamic characteristics of the p-channel JFET under the action of different electron fluences with energy $E_E = 4$ MeV at temperature $T = 303$ K and drain voltage $V_D = -4$ V. A positive voltage pulse ($V_G = 2$ V) of 3 µs duration is applied to the gate. The duration of the leading and trailing edges is 1 µs. From this figure we notice that up to fluence $F_E = 2 \cdot 10^{15}$ cm^{-2}, the duration dependence for the leading and trailing edges is practically identical. With further increasing the fluence, the trailing edge duration continues to decrease linearly up to 375 ns (change 13 % at $F_E = 6 \cdot 10^{15}$ cm^{-2}) The dependence of leading edge duration is nonlinear (decrease is less and equal to 5.7 %). The

difference can be explained by the effect of the drain current on the charge and capacitive discharge when the transistor is switched.

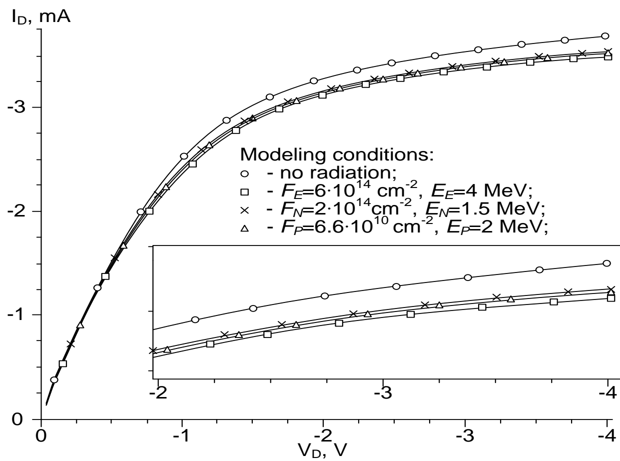


Fig. 9. Dependence of drain current I_D on drain voltage V_D at temperature 303 K under radiation

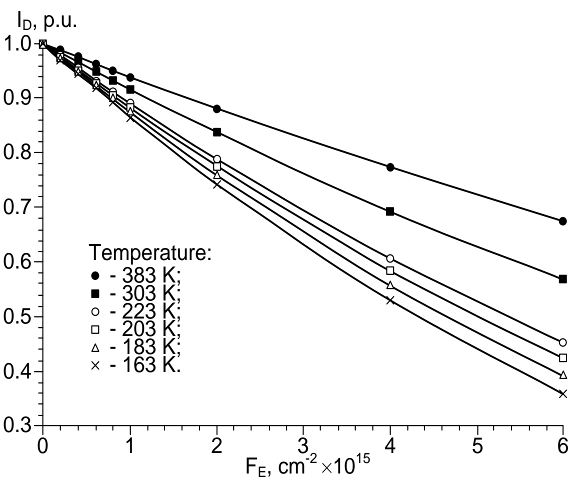


Fig. 10. Drain current as a function of electron fluence with energy E_E = 4 MeV at different temperatures

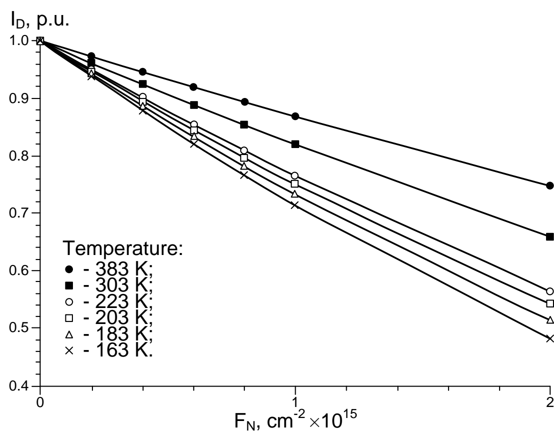


Fig. 11. Drain current as a function of neutron fluence with energy E_N = 1,5 MeV at different temperatures

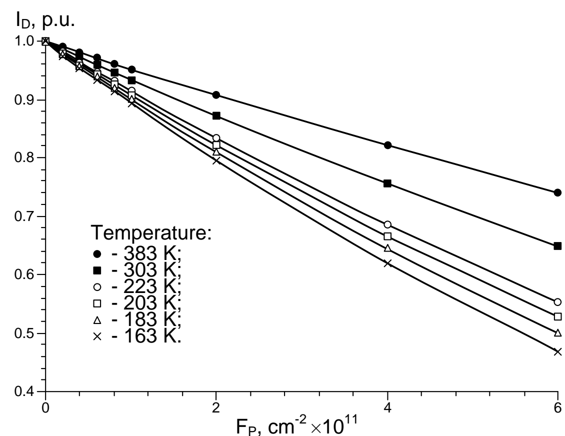


Fig. 12. Drain current as a function of proton fluence with energy E_P = 2 MeV at different temperatures

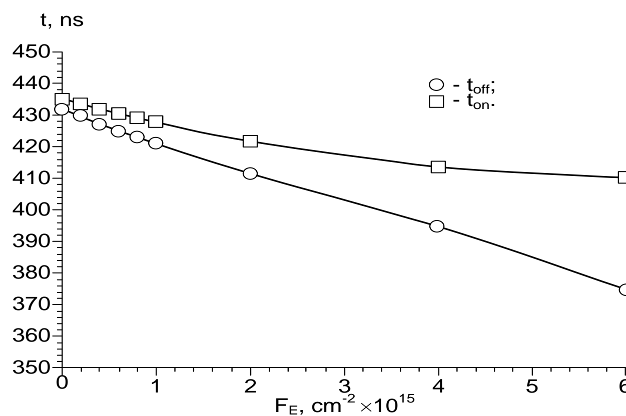


Fig. 13. Dependence of leading and trailing edge duration on electron fluence

Similar behavior is observed for neutron and proton fluxes. For the neutron flux with energy $E_N = 1.5$ MeV, the fluence value, at which the dependence of the leading edge duration becomes nonlinear, is $F_N = 8 \cdot 10^{14}$ cm^{-2}. For the proton flux with energy $E_P = 2$ MeV, this fluence equals $F_P = 2 \cdot 10^{11}$ cm^{-2}.

5. Simulation of n-channel JFET

The active region of device structure of the n-JFET is shown in Fig. 1b. The substrate has hole type conductivity, doped boron concentration of $1.35 \cdot 10^{15}$ cm^{-3}, crystallographic orientation is (111). For this device structure, the nominal values of the pinch-off voltage V_{Goff} and the drain current I_D are respectively minus 1.297 V and 0.025 A. In modeling the process for the n-JFET formation, 11 steps are conventionally identified: setting the substrate and selecting the reference grid, sequential formation of n-pocket areas, p^+-buried layer, epitaxy, formation of oxide insulation, p-well areas, n-collector, n-base, opening of areas for contacts (together with oxidation of the substrate surface), forming regions of p^+-emitter, n^+-emitter, metallization. In Table 2, the parameters of n-channel and p-channel JFETs obtained as a result of the computer and full-scale experiments are presented.

Table 2. Comparison of the results of computer and full-scale experiment

Temperature, K	Pinch-off voltage at a $I_D = 1$ μA, V		Drain current at $V_{GS} = 0$ V, $V_{DS} = 3$ V, mA	
	p-channel (measurement)	n-channel (modeling)	p-channel (measurement)	n-channel (modeling)
223	1.15	-1.188	4.4	24.65
303	1.29	-1.297	3.345	2455
383	1.425	-1.46	2.674	22.5

33 parameters are defined for the selected stages of technological process of the formation n-JFET (the parameter designation at a simulation is indicated in parentheses): boron concentration (X01) in the starting substrate, dose (X02) and energy (X03) of antimony ions during implantation #1, time (X04) and temperature (X05) of annealing after implantation #1, dose (X06) and energy (X07) of boron during implantation #2, time (X08) and temperature (X09) of annealing after implantation #2, thickness (X10) of epitaxial layer and concentration (X11) of phosphorus in it, time (X12) and temperature (X13) of thermal oxidation silicon, dose (X14) and energy (X15) of boron ions during implantation #3, time (X16) and temperature (X17) of annealing after implantation #3, dose (X18) and energy (X19) of phosphorus ions during implantation #4, time (X20) and temperature (X21) of annealing after implantation #4, dose (X22) and energy (X23) of phosphorus ions during implantation #5, time (X24) and temperature (X25) of annealing after implantation #5, dose (X26) and energy (X27) of boron ions during implantation #6, time (X28) and temperature (X29) of annealing after implantation #6, dose (X30) and energy (X31) of phosphorus ions during implantation #7, time (X32) and temperature (X33) of annealing after implantation #7.

We have modeled the dependence of drain current I_D of n-JFET on drain voltage V_D at gate voltage $V_G = 0$ V and impact of the neutron fluence $F_N = 2 \cdot 10^{14}$ cm^{-2} with energy $E_N = 1.5$ MeV for various technological operations. Analysis has shown that the most influence on the resistance to the neutron flux is due to the temperatures at which the technological operations of oxidation (X13) and annealing after implantation #3 (X17), #5 (X25), #6 (X29) and #7 (X33) are appeared.

Changing temperature (X09) of annealing after implantation #2, energy (X23) of phosphorus ions during implantation #5, dose (X26) and energy (X27) of boron ions during implantation #6, time (X32) of annealing after implantation #7 has a smaller influence on the

resistance of the device structure n-JFET. The remaining parameters practically have no effect on the drain current deviation under neutron radiation.

Figure 14 shows the drain current when parameters X13, X17, X25, X29, X33 being changed. Figure 15 displays the drain current deviation from an initial value for these parameters. All parameters have a significant effect on the drain current; when parameters X25 and X33 change from $0.9{\cdot}P_{nom}$ to $1.1{\cdot}P_{nom}$ the drain current I_D increases and decreases to three-fold, respectively.

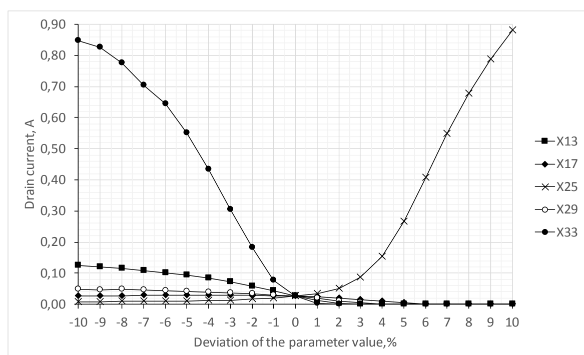


Fig. 14. Dependence of drain current on technological parameters of manufacturing n-JFET

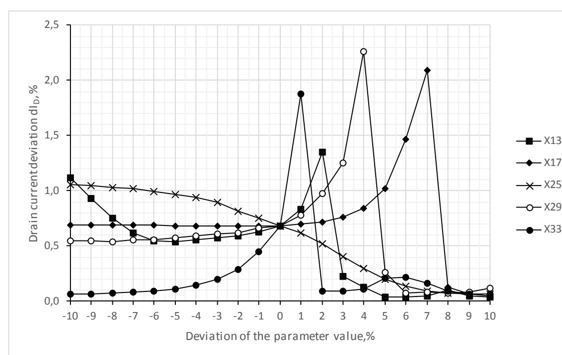
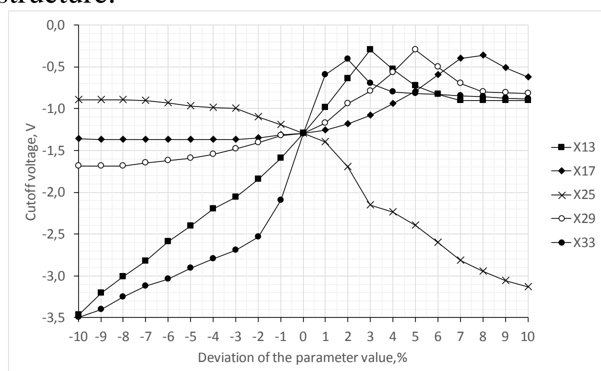


Fig. 15. Drain current deviation from a nominal value due to changing technological parameters

Figure 16 presents the pinch-off voltage V_{Goff} when parameters X13, X17, X25, X29, X33 being changed. All parameters have a significant effect on the pinch-off voltage; when the values of parameters is changed from $0.9{\cdot}P_{nom}$ to $1.1{\cdot}P_{nom}$, the pinch-off increases due to parameter X25 and decreases due to parameters X13 and X33 by more than four times. To increase hardness of device structure of n-JFET by optimizing design features and modes of technological operations, it is difficult to use parameters X13, X17, X25, X29, X33, because it is necessary to maintain the value of pinch-off voltage.

Using modified Levenberg-Marquardt algorithm for constructing the response surface describing relationship between the input parameters and the output characteristic in the iterative process, we obtained the modes of technological operations, providing a deviation of the drain current no more than 0.5 % when exposed to neutron fluence $F_N = 2{\cdot}10^{14}$ cm^{-2} with energy $E_N = 1.5$ MeV. For the optimized device structure, the nominal values of pinch-off voltage V_{Goff} and drain current I_D are respectively –1.312 V and 0.0252 A. Figure 17 show the drain current deviation under the action different neutron fluences for the initial and optimized structure.



Fig, 16. Dependence of pinch-off voltage on technological parameters at manufacturing n-JFET

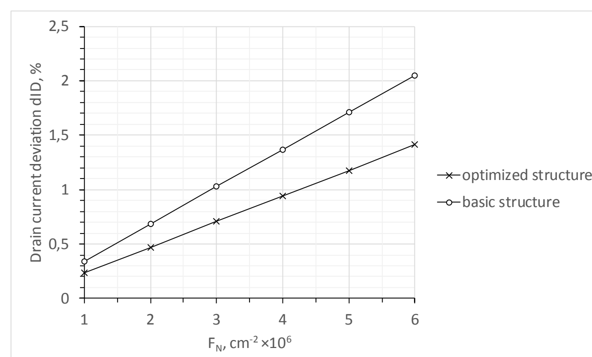


Fig. 17. Drain current deviation under radiation of neuron fluences at energy $E_N = 1.5$ MeV for the initial and optimized structures

It can be seen that for the optimized device structure, the effect of neutron flux with energy E_N = 1.5 MeV is reduced by 1.45 times; for the basic and optimized device structure of n-JFET, drain current deviation under neutron fluence $F_N = 1 \cdot 10^6$ cm^{-2} is equal to 0.34 % and 0.24 %, and under neutron fluence $F_N = 6 \cdot 10^6$ cm^{-2} equals 2.05 % and 1.41 %, respectively.

6. Conclusions

The results of modeling electrical characteristics of the device structure p-channel JFET showed acceptable agreement with experimental data in temperature range from 383 K to 223 K. Pinch-off voltage at temperature 303 K is 1.31 V (measured at 1.29 V), drain current is 3.9 mA (3.4 mA), for temperatures 383 K and 223 K the magnitude of these characteristics is 1.49 V (1.43 V) and 2.85 mA (2.7 mA), 1.17 V (1.15 V) and 4.58 mA (2.68 mA), respectively.

The series of computer experiments has verified the assumption [10] of the equality of degradation effect introduced by electron neutron and proton fluxes of fluences F_E with energy E_E = 4 MeV, $F_N = 0.302 \cdot F_E$ with energy E_N = 1.5 MeV, and $F_P = 1.1 \cdot 10^{-4}$ F_E with energy E_P = 2.0 MeV, respectively.

For the considered device structure p-channel JFET, it has been established that decreasing temperature increases the influence of electron flux.

Structural and technological parameters that have the greatest influence on deviation of the drain current I_D at the action of neutron fluence $F_N = 2 \cdot 10^{14}$ cm^{-2} with energy E_N = 1.5 MeV are determined. It is established that using electrical characteristics to optimize the resistance to neutron flux of n-JFET device, modes of the technological operations: thermal oxidation (parameter X13), annealing after implantation in the formation of p-well regions (X17), n-base (X25), p^+-emitter (X29), n^+-emitter (X33) lead to a spread of pinch-off voltage V_{Goff} and drain current I_D up to inoperability of the device.

Using modified Levenberg-Marquardt algorithm values modes of technological operations are obtained, providing the drain current deviation no more than 0.5 % when exposed to neutron fluence $F_N = 2 \cdot 10^{14}$ cm^{-2} with energy E_N = 1.5 MeV. For optimized device structure, nominal values of the pinch-off voltage V_{Goff} and drain current I_D are respectively – 1.312 V and 0.0252 A, the influence of neutron flux with energy E_N = 1,5 MeV reduced by 1.45 times in comparison with basic structure.

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